

METHOD AND RELATIVE CIRCUIT FOR INCREMENTING,
DECREMENTING OR TWO'S COMPLEMENTING A BIT STRING

Field of the Invention

[0001] The present invention relates to complementation devices used in microprocessors, and in particular, to a method and an associated circuit for incrementing, decrementing or two's complementing a bit string.

Background of the Invention

[0002] Generally, a microprocessor includes an Arithmetic and Logic Unit (ALU) for performing the four arithmetic operations. In the ALU, every integer number X is represented in the form of a bit string using the so-called two's complement coding. Indicating with X_k a generic bit of a string of N bits representing the number $X \in [-2^{N-1}, 2^{N-1} - 1]$, the integer number X is given by

$$X = \sum_{k=0}^{N-2} X_k \cdot 2^k - X_{N-1} \cdot 2^{N-1} \quad (1)$$

This coding is very convenient because it allows the difference operation to be performed as a sum of relative numbers using a common adder.

[0003] The two's complement of a bit string X may be easily obtained by logic circuits. In fact, indicating with \bar{X} the one's complement of X is given by

$$\bar{X} = 2^N - 1 - X \quad (2)$$

which is obtained by inverting each bit of the string X . The string $Y_{rc}(X)$ representing the two's complement of X is simply obtained adding 1 to the one's complement of X is given by

$$Y_{rc}(X) = \bar{X} + 1 = 2^N - X \quad (3)$$

[0004] A two's complement circuit is depicted in Figure 1. The two's complement circuit of the ALU may be used for performing increment or decrement operations. The circuit of Figure 2 increments by one the string X because the string $X+1$ is the two's complement of the one's complement of the string X is given by

$$X + 1 = \bar{\bar{X}} + 1 = (\bar{X}) + 1 = Y_{rc}(\bar{X}) \quad (4)$$

[0005] Similarly, it is possible to demonstrate that the circuit of Figure 3 decrements by one the string X , because the string $X-1$ is the one's complement of the two's complement of the string X is given by

$$X - 1 = 2^N - 2^N + X - 1 = 2^N - 1 - (2^N - X) = 2^N - 1 - Y_{rc}(X) = \overline{Y_{rc}(X)} \quad (5)$$

[0006] The fact that these increment and decrement operations can be performed by a two's complement circuit has lead to the realization of the so-called DIT (Decrement, Increment, Two's complement) circuits, such as the one depicted in Figure 4. This circuit is substantially formed by a logic selection circuit SEL

generating logic signals INV_IN and INV_OUT, by an array of input XOR gates input with the bits of the string X and the signal INV_IN, and by an array of XOR output gates receiving the bits of the two's complement string and the signal INV_OUT. The circuit of Figure 4 performs a decrement, increment or two's complement operation, with the logic state of the commands ID and TC being determined according to the following table

TABLE 1

ID	TC	OPERATION	INV_IN	INV_OUT
0	0	Decrement	0	1
1	0	Increment	1	0
-	1	two's	0	0

[0007] Because of the importance of the DIT circuit, the architecture thereof has been studied to find two's complement circuits that imply the smallest possible number of required elementary operations and that occupy the smallest possible silicon area. In the articles by R. Hashemian "Highly Parallel Increment/Decrement Using CMOS Technology", Proceedings of the 33rd Midwest Symposium on Circuits and Systems, Calgary, Alberta, Canada, August 12-14, 1990 and by R. Hashemian and C. Chen "A New Parallel Technique For Design of Decrement/Increment and Two's Complement Circuits", Proceedings of the 34th Midwest Symposium on Circuits and Systems, Monteray, California, May 14-17, 1991 techniques for forming decrement, increment and two's complement circuits are described, that offer certain advantages both in terms of silicon area consumption as well as in terms of speed.

[0008] By applying eq. 3, it is possible to note that the two's complement of the number -2^{N-1} is the

number -2^{N-1} itself. This fact is due to the asymmetry of the interval $X \in [-2^{N-1}, 2^{N-1}-1]$, thus the two's complement of -2^{N-1} exceeds the representation interval.

[0009] In many applications the two's complement of -2^{N-1} is represented with the positive integer $2^{N-1}-1$

$$Y_{RC}(-2^{N-1}) = 2^{N-1}-1 = \bar{X} \quad (6)$$

generating at the same time an overflow flag OF signaling that the representation interval has been exceeded.

[0010] A known two's complement circuit with overflow check is depicted in Figure 5. It generates an overflow flag OF when the string to be complemented represents the number -2^{N-1} , and has a correction circuit CLIP that receives a two's complement string Z and the overflow flag OF, generating the correct output string Y.

[0011] The overflow check circuit OVERFLOW CHECK is input with the string X and with a string REF representing the number -2^{N-1} , and activates the flag OF when the two strings coincide. The correction circuit CLIP generates an output string Y equal to the two's complement string Z when the flag OF is not active, while it produces the string 011...1 representing the number $2^{N-1}-1$ when the flag OF is active. Unfortunately, the known two's complement circuit depicted in Figure 5 is not convenient because the circuit OVERFLOW CHECK is an N bit comparator, whose silicon area occupation depends on the number of bits of the string X.

Summary of the Invention

[0012] In view of the foregoing background, an object of the present invention is to provide a method

and an associated circuit for incrementing, decrementing or two's complementing an N bit string X in a straightforward manner.

[0013] To perform these operations, the method of the invention generates an auxiliary string M of N bits as a function of the string X , and combines it logically with the string X to generate a corresponding output string Y . The least significant bit of the auxiliary string is independent from the bits of the string X , and any other bit M_L of the auxiliary string.

[0014] The operation of generating the auxiliary string M for performing the operations of increment, decrement and two's complement is particularly convenient for generating an overflow flag when the number to be output exceeds the representation interval. In fact, according to the method of the invention, an overflow flag OF is generated simply by combining logically the most significant bits M_{N-1} and X_{N-1} of the strings M and X . This is a great advantage because the overflow flag is generated by a single logic gate input with the bits M_{N-1} and X_{N-1} , independently from the number of bits N of the string X , while in known two's complement circuits it is generated by an N bit comparator that occupies a silicon area that is non-negligible and depends on the length of the string X .

[0015] Obviously, depending on the fact that an increment, decrement or two's complement operation is to be performed, the strings X and M are combined according to different logic operations for generating the output string Y .

[0016] The method of the invention is implemented by a circuit for incrementing, decrementing or two's complementing a string formed by a number of N bits.

The circuit comprises an auxiliary circuit generating an auxiliary string of N bits as a function of the first string. The least significant bit of the auxiliary string is independent from the first string and any other bit of the auxiliary string. The method starts from the second least significant bit up to the most significant bit, and performs a logic combination of a corresponding bit of the first string or of a negated replica thereof, starting from the least significant bit up to the second most significant bit, and of the bits of the first string or of the negated replica thereof less significant than the corresponding bit. Logic circuit means generate an output string as a logic combination of the auxiliary string and of the first string.

Brief Description of the Drawings

- [0017] The different aspects and advantages of the present invention will appear even more evident through a detailed description of embodiments referring to the attached drawings, wherein:
- [0018] Figure 1 depicts a two's complement circuit of a string according to the prior art;
- [0019] Figure 2 depicts an increment circuit of a string using a two's complement circuit according to the prior art;
- [0020] Figure 3 depicts a decrement circuit of a string using a two's complement circuit according to the prior art;
- [0021] Figure 4 depicts a multifunction DIT circuit without overflow check according to the prior art;
- [0022] Figure 5 depicts a two's complement circuit with overflow check according to the prior art;
- [0023] Figure 6a depicts a two's complement circuit

of the invention having an auxiliary circuit OR MASK;

[0024] Figure 6b depicts a two's complement circuit of the invention having an auxiliary circuit AND MASK;

[0025] Figure 7a is a detailed view of the auxiliary circuit depicted in Figure 6a;

[0026] Figure 7b is a detailed view of the auxiliary circuit depicted in Figure 6b;

[0027] Figure 8a is a detailed view of a second embodiment of the auxiliary circuit depicted in Figure 6a;

[0028] Figure 8b is a detailed view of a third embodiment of the auxiliary circuit of Figure 6a;

[0029] Figure 9a depicts a decrement circuit of the invention using the two's complement circuit of Figure 6a;

[0030] Figures 9b and 9c depict alternative embodiments of the decrement circuit of Figure 9a;

[0031] Figure 10a depicts an increment circuit of the invention that uses the two' complement circuit of Figure 6a;

[0032] Figures 10b and 10c depict alternative embodiments of the increment circuit of Figure 10a;

[0033] Figure 11a depicts an increment/decrement circuit of the invention that uses the circuit of Figure 6a;

[0034] Figures 11b, 11c and 11d depict alternative embodiments of the increment/decrement circuit of Figure 11a;

[0035] Figure 12a depicts a multifunction DIT circuit of the invention that uses the circuit of Figure 6a;

[0036] Figures 12b and 12c depict alternative embodiments of the multifunction DIT circuit of Figure 12a;

[0037] Figure 13 depicts a two's complement circuit of the invention with overflow test that uses the two's complement circuit of Figure 6a;

[0038] Figure 14 is a detailed view of the circuit of Figure 13;

[0039] Figure 15 depicts a multifunction DIT circuit of the invention with overflow check that uses the two's complement circuit of Figure 6a;

[0040] Figure 16 shows the functioning characteristics of a DIT circuit of the invention;

[0041] Figure 17 depicts a circuit for decrementing or two's complementing with overflow check that uses the two's complement circuit of Figure 6a, and has a correction circuit CLIP upstream the output array of XOR logic gates;

[0042] Figure 18 illustrates another multifunction DIT circuit of the invention with overflow check that uses the circuit of Figure 17;

[0043] Figure 19 depicts in detail an embodiment of the multifunction DIT circuit of Figure 18; and

[0044] Figure 20 depicts in detail another embodiment of the multifunction DIT circuit of Figure 18.

Detailed Description of the Preferred Embodiments

[0045] Two equivalent embodiments of two's complement circuits implementing the method of the invention are depicted in Figures 6a and 6b. They have an auxiliary circuit OR MASK and AND MASK, respectively, input with the $N-1$ least significant bits of the string X and generating a corresponding auxiliary string M and \bar{M} of N bits.

[0046] It is worth noting that the auxiliary string \bar{M} generated by the circuit AND MASK is a negated

version of the string M generated by the circuit OR MASK. The two circuits of Figures 6a and 6b are thus nearly equivalent.

[0047] According to the method of the invention, with X_{L-1} being the least significant bit X of the string X equal to 1, the least significant bits of the auxiliary string from the second M_1 to the $(L+1)$ -th M_L generated by the circuit of Figure 6a (or 6b) coincide with the L least significant bits of the string X (or with their negated replicas), while the remaining bits are all equal to 1 (or to 0), while the least significant bit of the auxiliary string M is independent from the string X and is 0 (or 1).

[0048] The circuit of Figure 6a effectively performs the two's complement of the string X . From simple calculations one finds that the two's complement (eq. 3) of the string X is the logic XOR between the string X and the string M

$$Y_{TC}(X) = X \oplus M \quad (7)$$

An auxiliary circuit OR MASK that is easy to form is shown in Figure 7a. It is substantially composed of an array of OR gates in cascade, with each gate being input with a bit of the string X and with the output of the OR gate that precedes in the cascade.

[0049] An auxiliary circuit AND MASK for the two's complement circuit of Figure 6b is depicted in Figure 7b. It is substantially similar to the circuit of Figure 7a but it has AND gates instead of OR gates and generates an auxiliary string \bar{M} which is the negated replica of the auxiliary string M generated by the circuit of Figure 7a.

[0050] As will be evident to those skilled in the

art, it is possible to form the circuits of Figures 7a and 7b even using NOR and NAND gates instead of OR and AND gates.

[0051] The auxiliary circuit OR MASK (AND MASK) is substantially a circuit that generates a string M whose L least significant bits are equal to 0(1) and all the remaining bits are equal to 1 (0), with X_{L-1} being the least significant bit equal to 1 of the string X . Therefore, it is evident that the auxiliary circuit of Figure 7a (7b) may be substituted by any other circuit that carries out the same operation. For example, it is possible to substitute the circuit of Figure 7a, which has OR gates in series, with auxiliary circuits OR MASK of Figure 8a and 8b, that have OR gates disposed in parallel and in a hybrid series-parallel structure, respectively. Alternative structures, similar to those of Figures 8a and 8b, may also be simply realized for the auxiliary circuit AND MASK of Figure 7b.

[0052] For better illustrating the invention, in the ensuing description reference will be made to the embodiment of Figure 6a with the auxiliary circuit OR MASK of Figure 7a, but what will be stated can be easily repeated even for the embodiment of Figure 6b and for all other embodiments of the auxiliary circuit.

[0053] The two's complement circuit of the invention may be used for forming a circuit for decrementing, depicted in Figure 9a, a circuit for incrementing, depicted in Figure 10a, an increment/decrement circuit depicted in Figure 11a, or finally a multifunction DIT circuit, depicted in Figure 12a. Alternative embodiments of decrement, increment, increment/decrement and multifunction DIT circuits equivalent to those of Figures 9a, 10a, 11a and 12a are depicted in Figures 9b and 9c, in Figures 10b and 10c, in Figures

from 11b to 11d and in Figures 12b and 12c,
respectively.

[0054] The truth table of signals ID, TC, INV_IN and
INV_OUT is TABLE 1 and the logic selection circuit SEL
of Figures from 12a to 12c is the same of Figure 4.

[0055] The method of the invention allows the
generation of the overflow flag simply as a logic
combination only of the most significant bits M_{N-1} and
 X_{N-1} of the auxiliary string M and of the string to be
complemented X, respectively, independently from the
number N of bits of the string to be complemented. A
two's complement circuit of the invention with overflow
check is depicted in Figure 13. The circuit OVERFLOW
CHECK can generate the overflow flag OF only using the
most significant bits X_{N-1} and M_{N-1} because when the
string X represents the number -2^{N-1} , and only in this
case, the bit X_{N-1} is 1 and the bit M_{N-1} is 0.

[0056] A great advantage of the present invention
with respect to the known two's complement circuit of
Figure 5 includes the fact that the overflow flag OF is
generated independently from the number N of bits of
the string X, and the circuit OVERFLOW CHECK occupies a
silicon area smaller than the area of an N bit
comparator.

[0057] A detailed scheme of an embodiment of a two's
complement circuit of the invention that performs the
correction of eq. 6 is depicted in Figure 14. The XOR
gate input with the bits X_0 and M_0 has been omitted
because the least significant bit of the auxiliary
string M_0 is always 0, and thus this gate is
unnecessary.

[0058] Moreover the gate of the two's complement
circuit input with the most significant bits M_{N-1} and
 X_{N-1} and generating the bit Z_{N-1} is an OR gate and not a

XOR gate, in order to correct the output when the string X to be complemented represents the number -2^{N-1} . In fact, independently from the state of the flag OF, the most significant bit Y_{N-1} of the output string may be generated by negating the bit Z_{N-1} , as it is evident from the following table:

TABLE 2

X	M_{N-1}	X_{N-1}	Y_{N-1}	Z_{N-1}
0...0	0	0	0	1
-2^{N-1}	0	1	0	1
any other	1	-	$\overline{X_{N-1}}$	X_{N-1}

[0059] The two's complement circuit with overflow test of Figure 13 may be used for realizing a multifunction DIT circuit of the invention for decrementing, incrementing and two's complementing, as depicted in Figure 15, whose circuit blocks are the same as that of Figures 4 and 13. It is easy to demonstrate that the features that describe the functioning of the DIT circuit of Figure 15 are that depicted in Figure 16.

[0060] Figure 17 depicts a general diagram of a preferred embodiment of a two's complement or decrement circuit of the invention. As it is possible to note, differently from the multifunction DIT circuit of Figure 15, the correction circuit CLIP is upstream the array of output XOR gates and is not input with a bit string but only with two signals, INV_OUT and OF, whichever the number N of bits of the string K is.

[0061] The correction circuit CLIP generates a correction signal INVCLIP and a negated replica of the signal INV_OUT for making the array of output XOR gates perform the correction of eq. 6 of the complemented

string Z . Therefore, the array of output XOR gates of the two's complement or decrement circuit of the invention is useful also when no decrement operation has been requested. This expedient allows a simplification of the structure of the correction circuit CLIP with a further saving of silicon area.

[0062] The two's complement or decrement circuit of the invention may be embodied in a multifunction DIT circuit for incrementing, decrementing or two's complementing a string as shown in Figure 18. The truth table of signals INV_IN and INV_OUT is TABLE 1, already written referring to the multifunction DIT circuit of Figure 4.

[0063] A detailed scheme of an embodiment of the multifunction DIT circuit of Figure 18 is depicted in Figure 19. In this embodiment, which is even more convenient than that of Figure 15, the overflow flag OF is generated by ANDing the most significant bit of the string to be two's complemented K_{N-1} and a negated replica of the most significant bit of the auxiliary string M_{N-1} , and the correction signal INVCLIP is the logic XOR between the overflow flag OF and the signal INV_OUT.

[0064] The circuit of Figure 19 performs the same functions of that of Figure 15. Should an overflow occur (OF=1), it would mean that the string K to be complemented represents the number -2^{N-1} , and thus the most significant bit Z_{N-1} of the complemented string is 1 while all other bits are 0. In the case in which any decrement operation has been required (INV_OUT=0), the correction signal INVCLIP is 1 and thus the $N-1$ least significant bits of the output string Y are 1 while the most significant bit Y_{N-1} is 0. In the case in which a decrement operation has been required (INV_OUT=1), the

correction signal INVCLIP is 0 and the output string Y is equal to the complemented string Z.

[0065] It is possible to verify immediately that, in all other possible cases, the operating characteristics of the DIT circuit of Figure 19 are that depicted in Figure 16. An embodiment of the invention, alternative to that of Figure 19, is depicted in Figure 20. The comprehension of its functioning is immediate and will not be described in detail.